

### ***Remarks***

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing remarks, claims 1-20, 32, and 35-40 are pending in the application, with 1, 11, and 32 being the independent claims.

Based on the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

### ***Statutory Double Patenting***

Claim 33 stands rejected under 35 U.S.C. § 101 as allegedly claiming the same invention as that of claim 31 of U.S. Patent No. 6,653,966 to van der Goes et al. (herein "van der Goes"). Applicants respectfully traverse the rejection.

Claim 33 may be literally infringed without literally infringing claim 31 of van der Goes. Claim 33 recites a method of converting an analog voltage to a digital voltage including the step of "converting outputs of the first and second amplifiers to *a digital output.*" (*emphasis added, see, claim 33*). On the other hand, claim 31 of van der Goes recites a method of converting an analog voltage to a digital voltage including the step of "converting outputs of the first and second amplifiers to *an N-bit output.*" (*see, van der Goes, col. 11, line 25 through col. 12, line 15*).

A digital output has a broader connotation than an N-bit output. A digital output represents a signal whose amplitude can take on any finite number of discrete values, whereas an N-bit output represents N-binary digits whose amplitude can take on a value of either 0 or 1. In other words, the N-bit output recited by claim 31 of van der Goes is a subset of the digital output recited by claim 33. For example, a digital signal whose

amplitudes can take on M values is an M-ary signal, of which binary (M=2) is a special case. Therefore, identical subject matter is not defined by both claims and statutory double patenting does not exist. (*see*, MPEP § 804). Accordingly, Applicants respectfully request this rejection be reconsidered and withdrawn.

***Allowed Claims***

Applicants thank the Examiner for indicating the allowability of claims 1-20, 32, and 35-40 in the Office Action dated April 19, 2007 (herein "Office Action").

***Comments on Statement of Reasons for Allowance***

Applicants note the Examiner's Statement of Reasons for Allowance presented on page 3 of the Office Action. Applicants reserve the right to demonstrate claims 1-20, 32, and 35-40 are allowable over the art made of record for further reasons related to any of their recited features. Applicants further contend that reservation of this right does not give rise to any implication regarding whether the Applicants agree with or acquiesce in the reasoning provided by the Examiner.

***Other Matters***

Applicants have identified the instant application as a continuation of Application No. 10/359,201, filed on February 6, 2003, entitled "Subranging Analog to Digital Converter with Multi-Phase Clock Timing." The Examiner did not indicate in prior communications that the cited references in Application No. 10/359,201 have been reviewed. Accordingly, Applicants' respectfully request the Examiner to initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered. (*see*, MPEP § 2001.06(b)).

***Conclusion***

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,

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